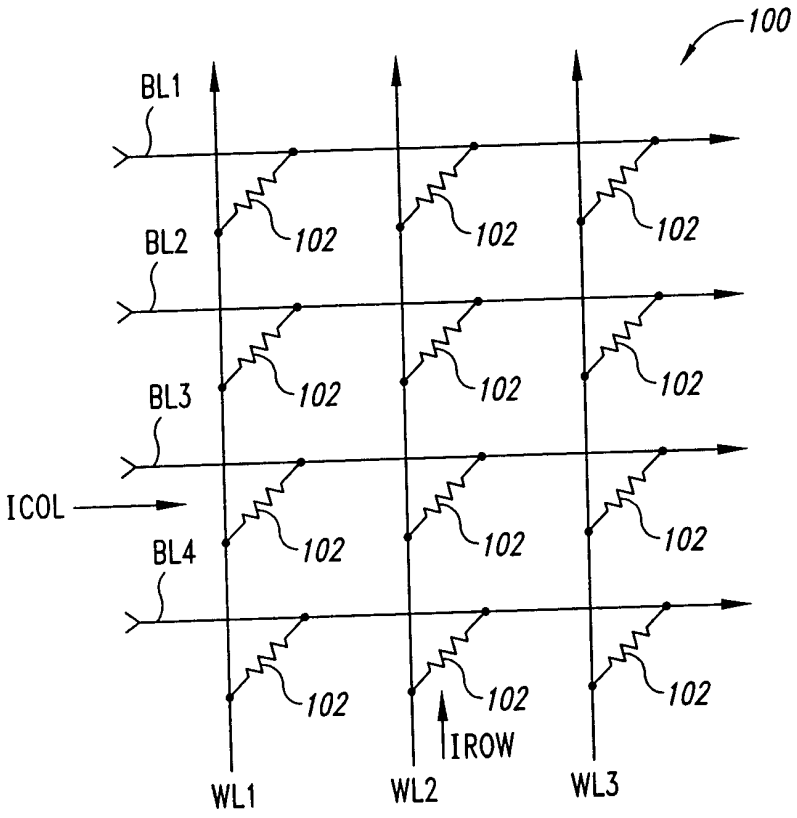

Fig. 1
(Background Art)

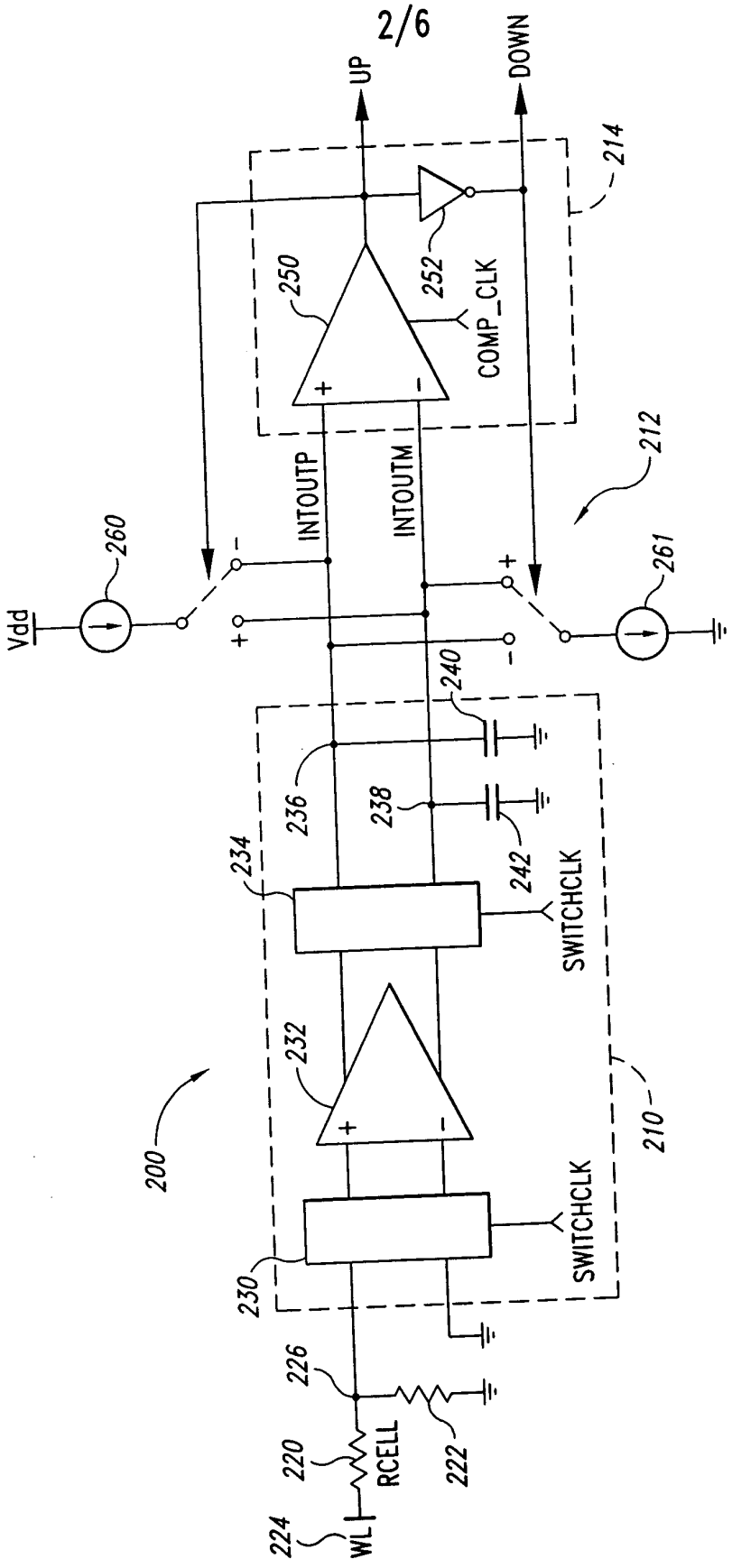
UP
DOWN
214
250
252
COMP_CLK
212
INTOUTP
INTOUTM
260
261
Vdd
240
236
238
242
234
SWITCHCLK
232
200
210
230
SWITCHCLK
226
220
RCELL
222
224
WL

Fig. 2

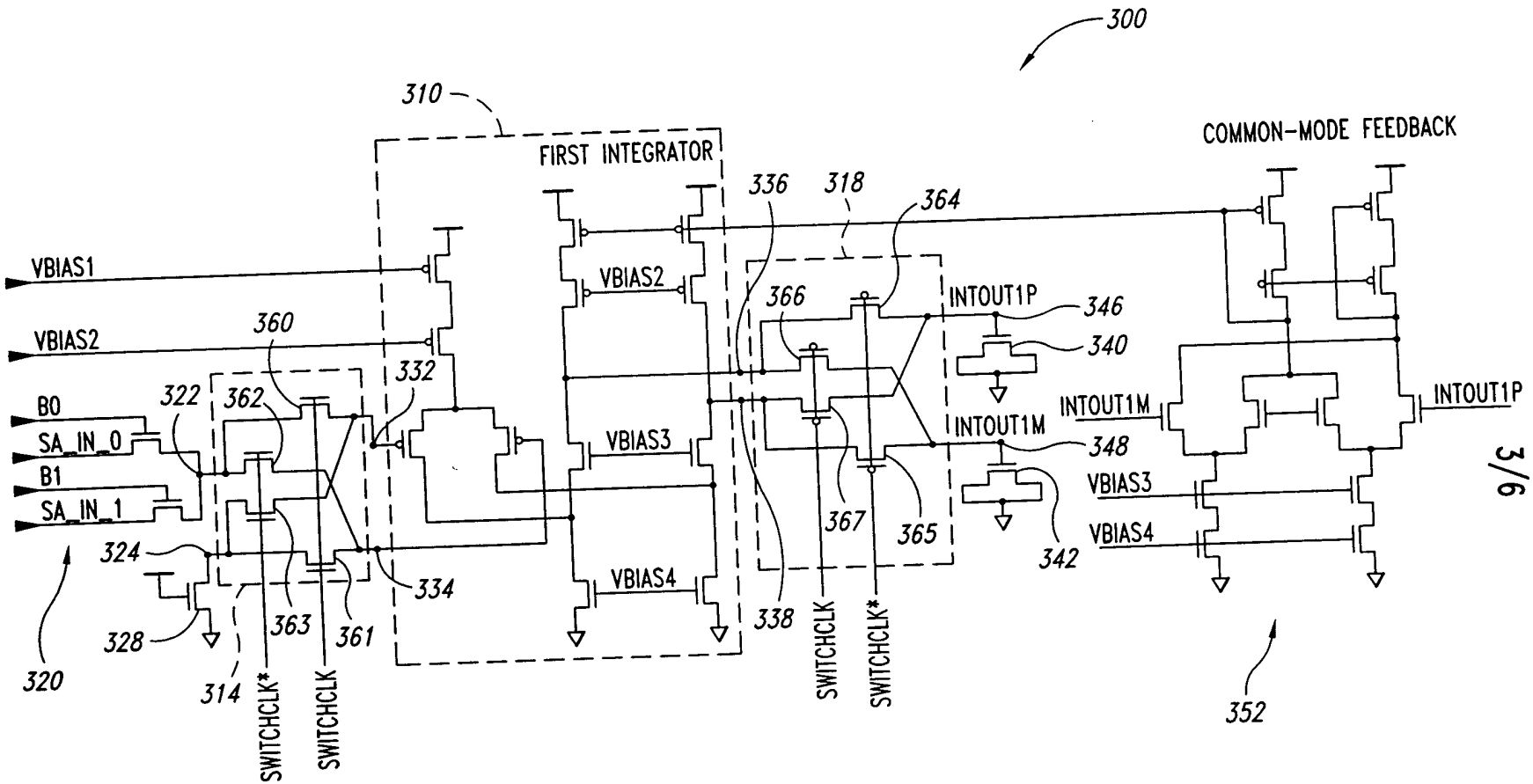
300
310
FIRST INTEGRATOR
COMMON-MODE FEEDBACK
VBIAS1
VBIAS2
B0
SA_IN_0
B1
SA_IN_1
VBIAS2
VBIAS3
VBIAS4
INTOUT1P
INTOUT1M
INTOUT1M
INTOUT1P
VBIAS3
VBIAS4
SWITCHCLK*
SWITCHCLK
SWITCHCLK
SWITCHCLK*
320
322
324
328
314
360
362
363
361
332
334
336
318
364
366
338
367
365
346
340
348
342
352

Fig. 3

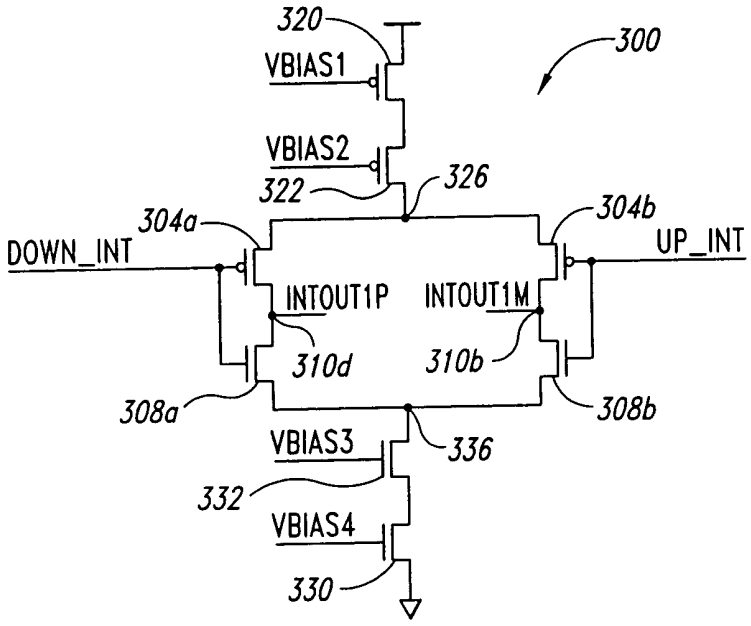
320
VBIAS1
300
VBIAS2
322
326
304a
304b
DOWN_INT
UP_INT
INTOUT1P
INTOUT1M
310d
310b
308a
308b
VBIAS3
336
332
VBIAS4
330

Fig. 4

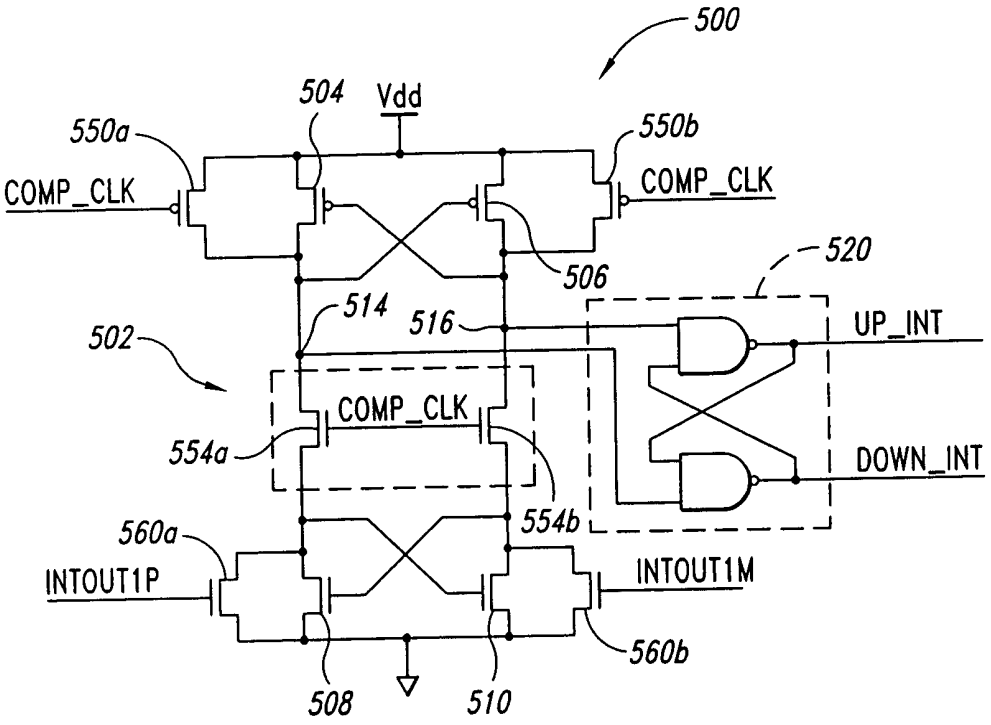
500
504
Vdd
550a
550b
COMP_CLK
COMP_CLK
506
520
514
516
UP_INT
502
COMP_CLK
554a
DOWN_INT
554b
560a
INTOUT1P
INTOUT1M
560b
508
510

Fig. 5

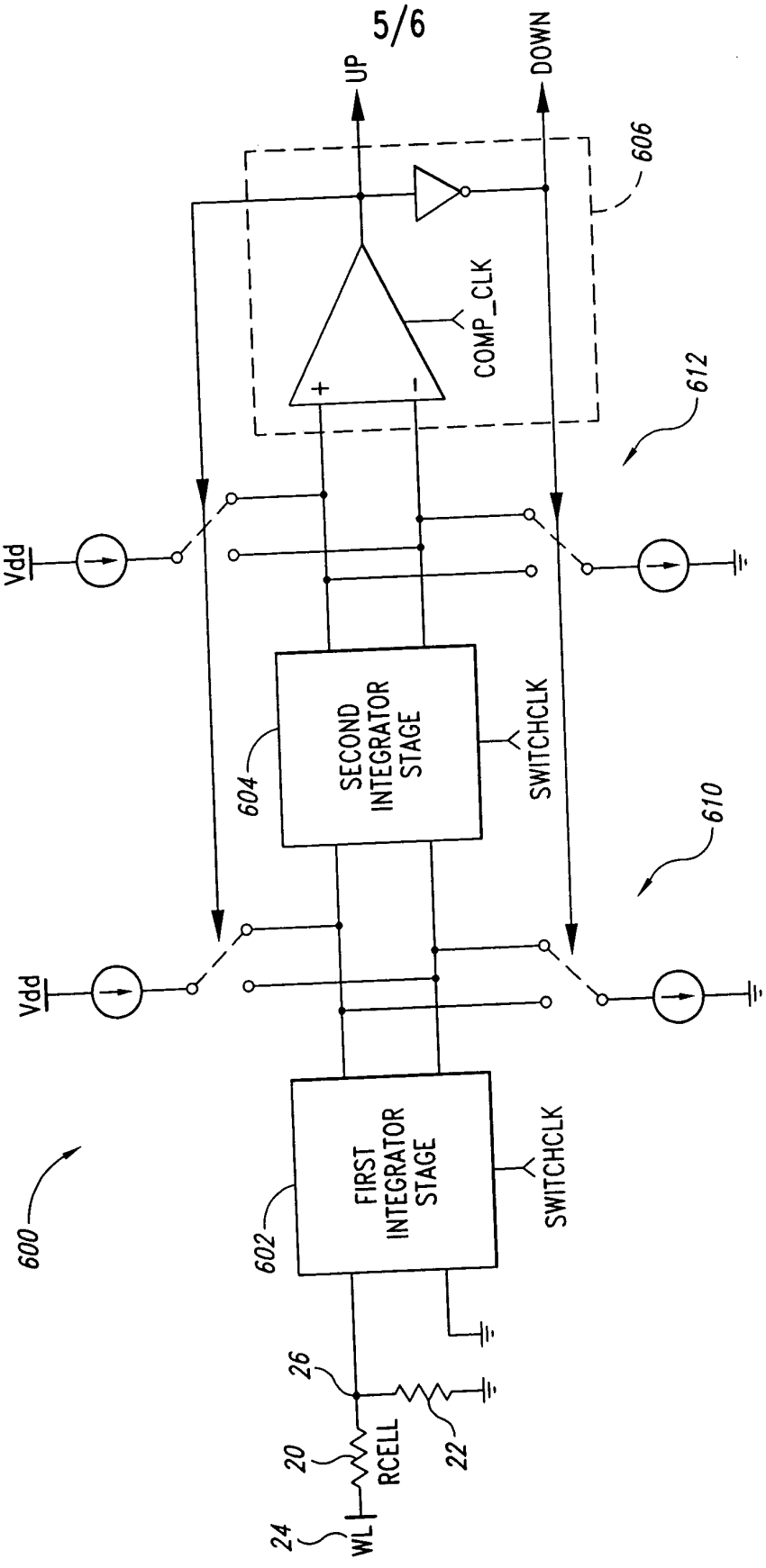
UP
DOWN
606
COMP_CLK
+
-
612
Vdd
SECOND INTEGRATOR STAGE
604
SWITCHCLK
610
Vdd
FIRST INTEGRATOR STAGE
602
SWITCHCLK
600
26
20
RCELL
22
24
WL

Fig. 6

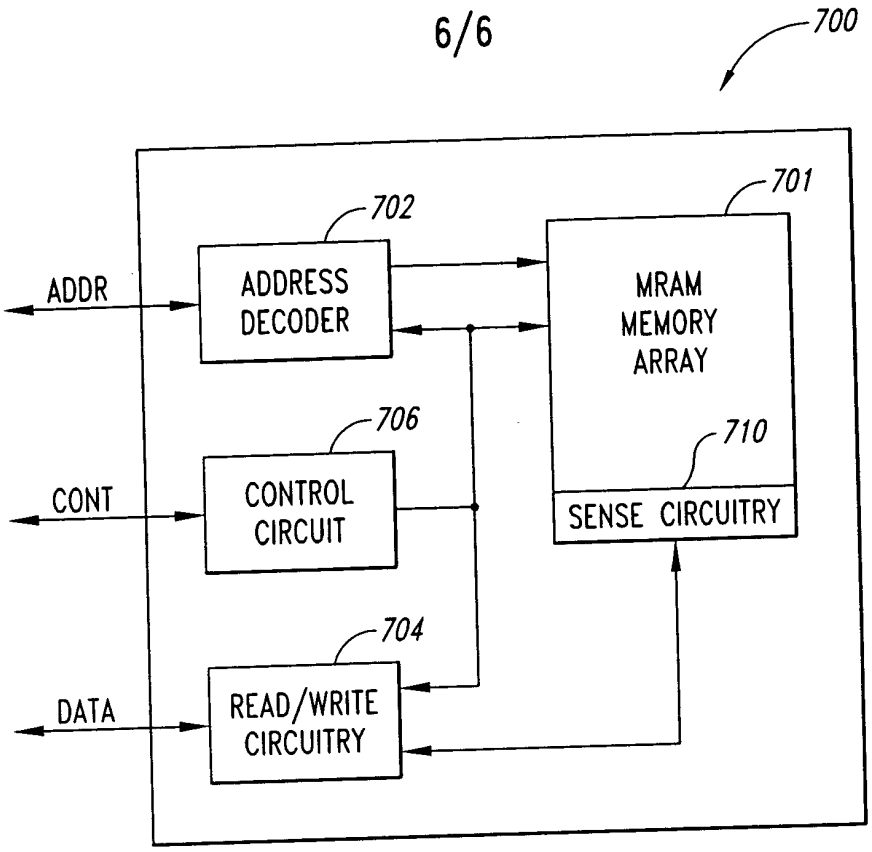
700
701
702
ADDR
ADDRESS DECODER
MRAM MEMORY ARRAY
706
710
CONT
CONTROL CIRCUIT
SENSE CIRCUITRY
704
DATA
READ/WRITE CIRCUITRY

Fig. 7

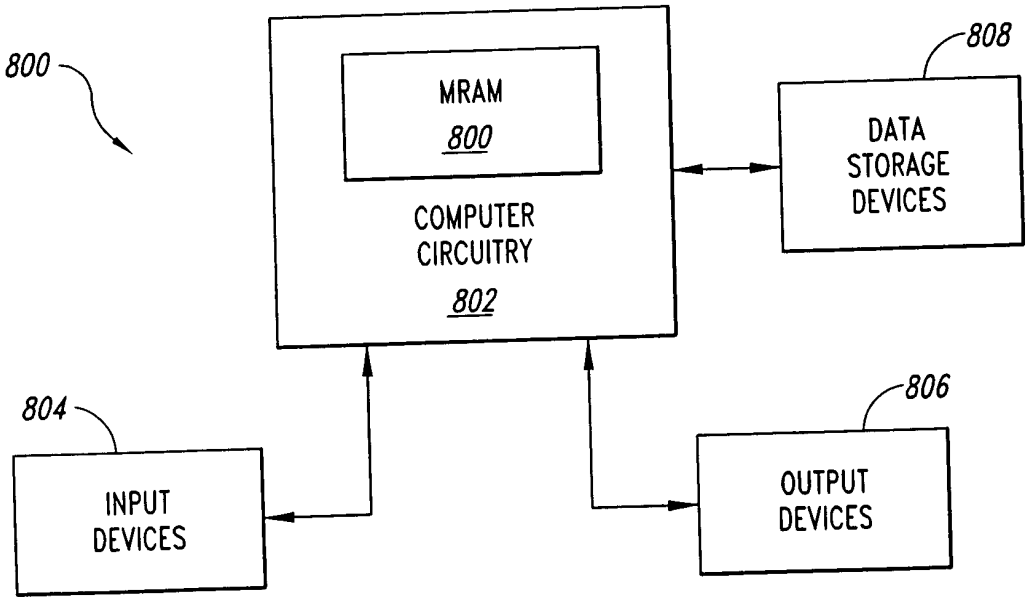
800
MRAM
800
COMPUTER CIRCUITRY
802
808
DATA STORAGE DEVICES
804
INPUT DEVICES
806
OUTPUT DEVICES

Fig. 8